

Fig. 1 IGBT with Monolithic or Discrete Diode Collector to Gate Clamp Circuit

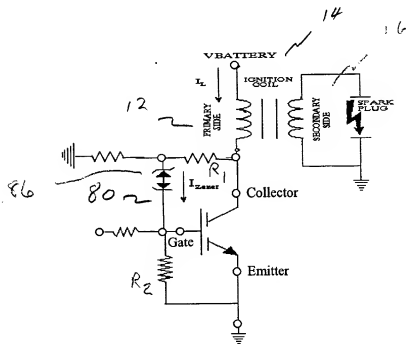


Fig. 2 IGBT with Monolithic or Discrete Resistive Voltage Divider and Diode Collector to Gate Clamp Circuit

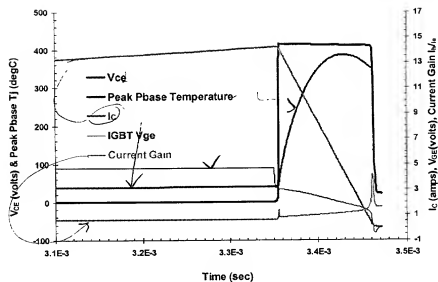


Fig. 3 Simulated 14.2A, 310mJ SCIS stress for and IGBT used in the circuit of Fig 1.

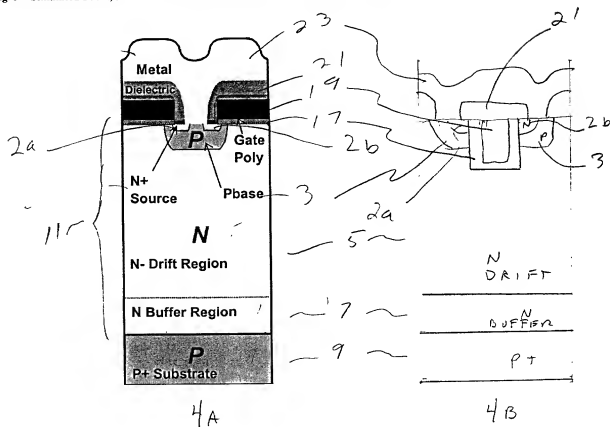


Fig. 4 Typical IGBT stripe cell vertical cross-section .

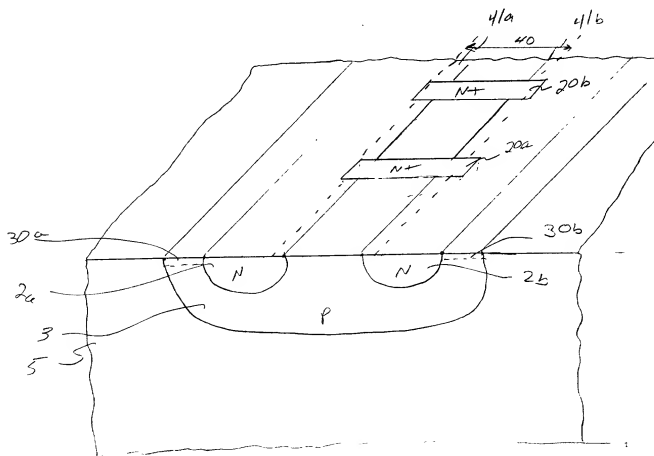
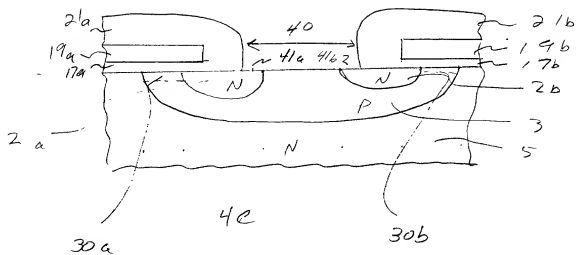


Fig. 5 Top view of stripe with full channel design . Contact to N Channel doping is along the entire length of the stripe.

A cross-sectional view of a semiconductor device structure. The structure consists of a central channel region (200) flanked by two side regions (205L and 205R). The channel region (200) contains a central layer (200C) and two side layers (200L and 200R). The side regions (205L and 205R) are doped with N-type dopants (N Doping). The central layer (200C) is labeled "N_{0.01} C_{0.01}". The side layers (200L and 200R) are labeled "200L" and "200R". The central region (200) is labeled "200". The side regions (205L and 205R) are labeled "205L" and "205R". The top surface is labeled "3". The bottom surface is labeled "Poly Opening". The right side is labeled "N JFET Region".

Fig. 6 Top view of stripe with channel version A exclude design. Top half of stripe separate N+ contacts. Bottom half of stripe continuous N+ contacts across the contact opening.

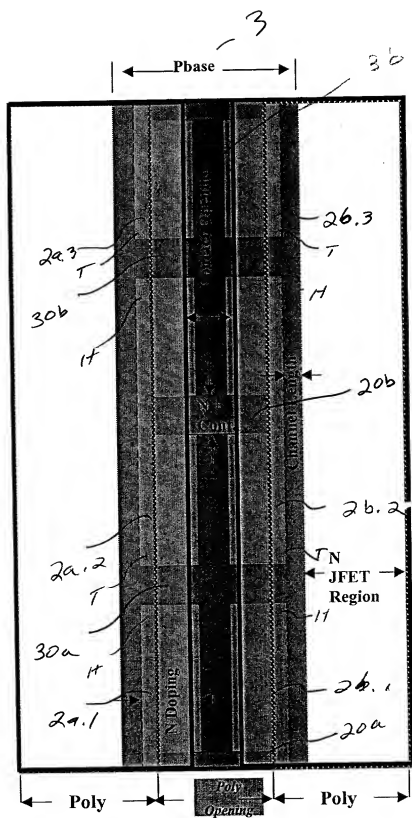


Fig. 7 Top view of stripe with Version B channel exclude design.

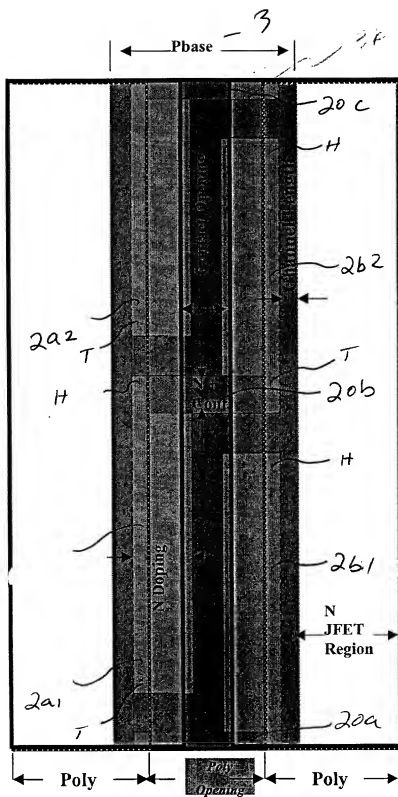


Fig. 8 Top view of stripe with Version C channel exclude design.

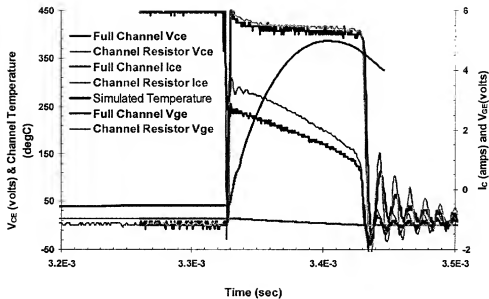


Fig. 10 Measured 27°C, 14.2A, $V_{ge}=5V$, $R_{ge}=1k\Omega$ SCIS Stress for full channel design in Fig 5 and invention shown in Fig 14 with channel resistor having equivalent active area..

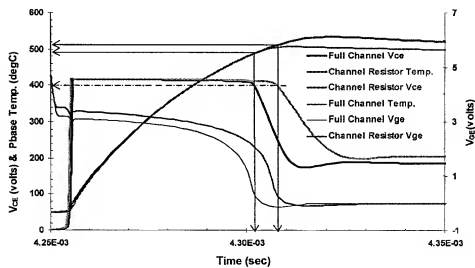


Fig. 11 Simulated 27°C, 17.8A, $V_{ge}=5V$, $R_{ge}=1k\Omega$ SCIS Stress for full channel design in Fig 5 and invention shown in Fig 14 with non-temperature compensated channel resistor having equivalent active area..

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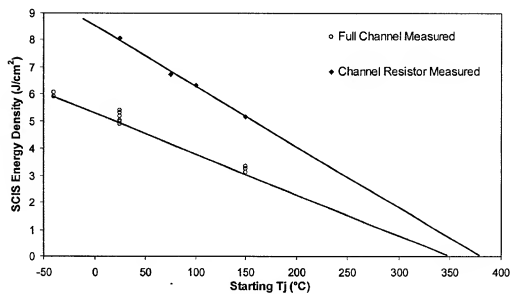


Fig. 12 Measured SCIS energy density capability with primary inductance of 3mH.

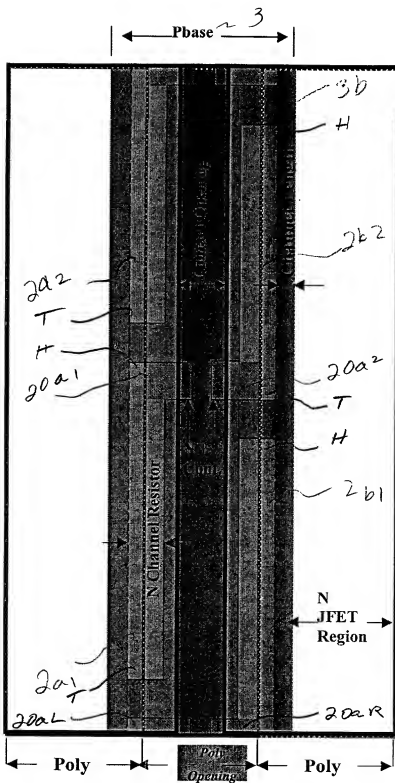
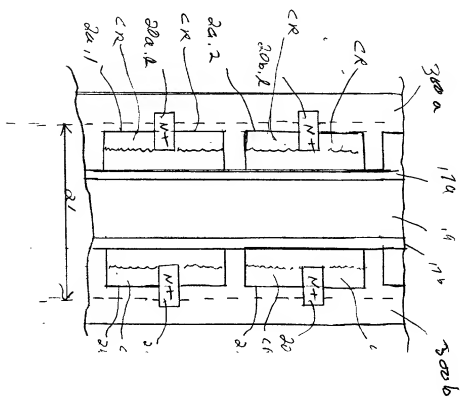
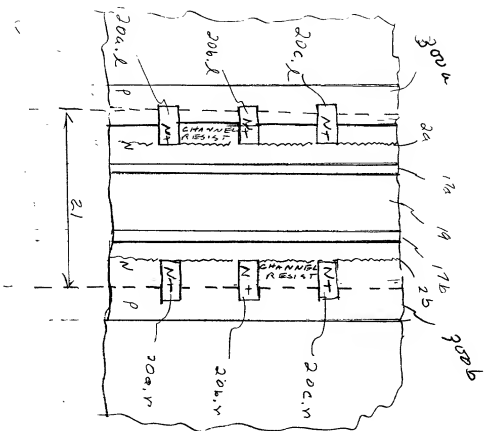


Fig. 14 Top view of stripe "H" pattern channel resistor design.



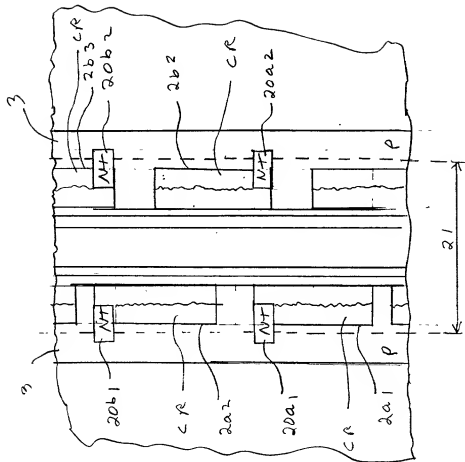


Fig. 17